REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

Prepared in accordance with ASME Y14.24

Vendor item drawing

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PMIC N/A	**PREPARED BY** Phu H. Nguyen	**DLA LAND AND MARITIME** **COLUMBUS, OHIO 43218-3990** **http://www.landandmaritime.dla.mil/**
Original date of drawing YY MM DD 12-11-08	**CHECKED BY** Phu H. Nguyen	**TITLE** MICROCIRCUIT, LINEAR, LOW POWER, RAIL TO RAIL, OUTPUT PRECISION JFET AMPLIFIER, MONOLITHIC SILICON
	APPROVED BY Thomas M. Hess	
	SIZE **A** **CODE IDENT. NO.** **16236**	**DWG NO.** **V62/12653**
	REV	**PAGE** 1 **OF** 8

AMSC N/A

5962-V024-13

1. SCOPE

1.1 Scope. This drawing documents the general requirements of a high performance low power, rail-to-rail, output precision JFET amplifier microcircuit, with an operating temperature range of -55°C to +125°C.

1.2 Vendor Item Drawing Administrative Control Number. The manufacturer's PIN is the item of identification. The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation:

V62/12653	-	01	X	E
Drawing number		Device type (See 1.2.1)	Case outline (See 1.2.2)	Lead finish (See 1.2.3)

1.2.1 Device type(s).

Device type	Generic	Circuit function
01	AD8643-EP	Low power, rail-to-rail, output precision JFET amplifier

1.2.2 Case outline(s). The case outlines are as specified herein.

Outline letter	Number of pins	JEDEC PUB 95	Package style
X	14	JEDEC MS-012-AB	Standard Small Outline Package

1.2.3 Lead finishes. The lead finishes are as specified below or other lead finishes as provided by the device manufacturer:

Finish designator	Material
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
Z	Other

1.3 Absolute maximum ratings. 1/

Supply voltage ..... 27.3 V
Input voltage ..... V- to V+
Differential input voltage ..... ±Supply voltage
Output short circuit duration ..... Indefinite
Operating temperature range: ..... -55°C to +125°C
Storage temperature range ..... -65°C to 150°C
Junction temperature ..... -65°C to 150°C
Lead temperature (Soldering, 60 sec) ..... 300°C

1.4 Thermal characteristics.

Thermal resistance

Case outline	θ_{JA}	θ_{JC}	Unit
Case X	120	36	°C/W

2. APPLICABLE DOCUMENTS

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP95 – Registered and Standard Outlines for Semiconductor Devices

(Copies of these documents are available online at http:/www.jedec.org or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201.)

3. REQUIREMENTS

3.1 Marking. Parts shall be permanently and legibly marked with the manufacturer's part number as shown in 6.3 herein and as follows:

A. Manufacturer's name, CAGE code, or logo
B. Pin 1 identifier
C. ESDS identification (optional)

3.2 Unit container. The unit container shall be marked with the manufacturer's part number and with items A and C (if applicable) above.

3.3 Electrical characteristics. The maximum and recommended operating conditions and electrical performance characteristics are as specified in 1.3, and table I herein.

3.4 Design, construction, and physical dimension. The design, construction, and physical dimensions are as specified herein.

3.5 Diagrams.

3.5.1 Case outline. The case outline shall be as shown in 1.2.2 and figure 1.

3.5.2 Terminal connections. The terminal connections shall be as shown in figure 2.

1/ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

TABLE I. Electrical performance characteristics. 1/

Test	Symbol	Test conditions V_S = 5.0 V, V_{CM} = 2.5 V T_A = 25°C unless otherwise noted	Limits			Unit
			Min	Typ	Max	
Input characteristics						
Offset voltage	V_{OS}			50	1000	µV
		-55°C < T_A < +85°C			1.8	mV
		+85°C < T_A < +125°C , V_{CM} = 1.5 V			1.9	mV
Input bias current	I_B			0.25	1	pA
		-55°C < T_A < +125°C			180	
Input offset current	I_{OS}				0.5	
		-55°C < T_A < +125°C			60	
Input voltage range			0		3	V
Common mode rejection ratio	CMRR	V_{CM} = 0 V to 2.5 V	74	93		dB
Large signal voltage gain	A_{VO}	R_L = 10 kΩ, V_O = 0.5 V to 4.5 V	80	140		V/mV
Offset voltage drift	$\Delta V_{OS}/\Delta T$	-55°C < T_A < +125°C		2.5		µV/°C
Output characteristics						
Output voltage high	V_{OH}		4.95			V
		I_L = 1 mA, -55°C to +125°C	4.94			
Output voltage low	V_{OL}				0.05	
		I_L = 1 mA, -55°C to +125°C		0.01	0.05	
Output current	I_{OUT}			±6		mA
Power supply						
Power supply rejection ratio	PSRR	V_S = 5 V to 26 V	90	107		dB
Supply current/Amplifier	I_{SY}			195	250	µA
		-55°C < T_A < +125°C			270	
Dynamic performance						
Slew rate	SR			2		V/µs
Gain bandwidth product	GBP			2.5		MHz
Phase margin	$ø_m$			50		Degrees
Noise performance						
Voltage noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.0		µV p-p
Voltage noise density	e_N	f = 1 kHz		28.5		nV/√Hz
Current noise density	i_N	f = 1 kHz		0.5		fA/√Hz

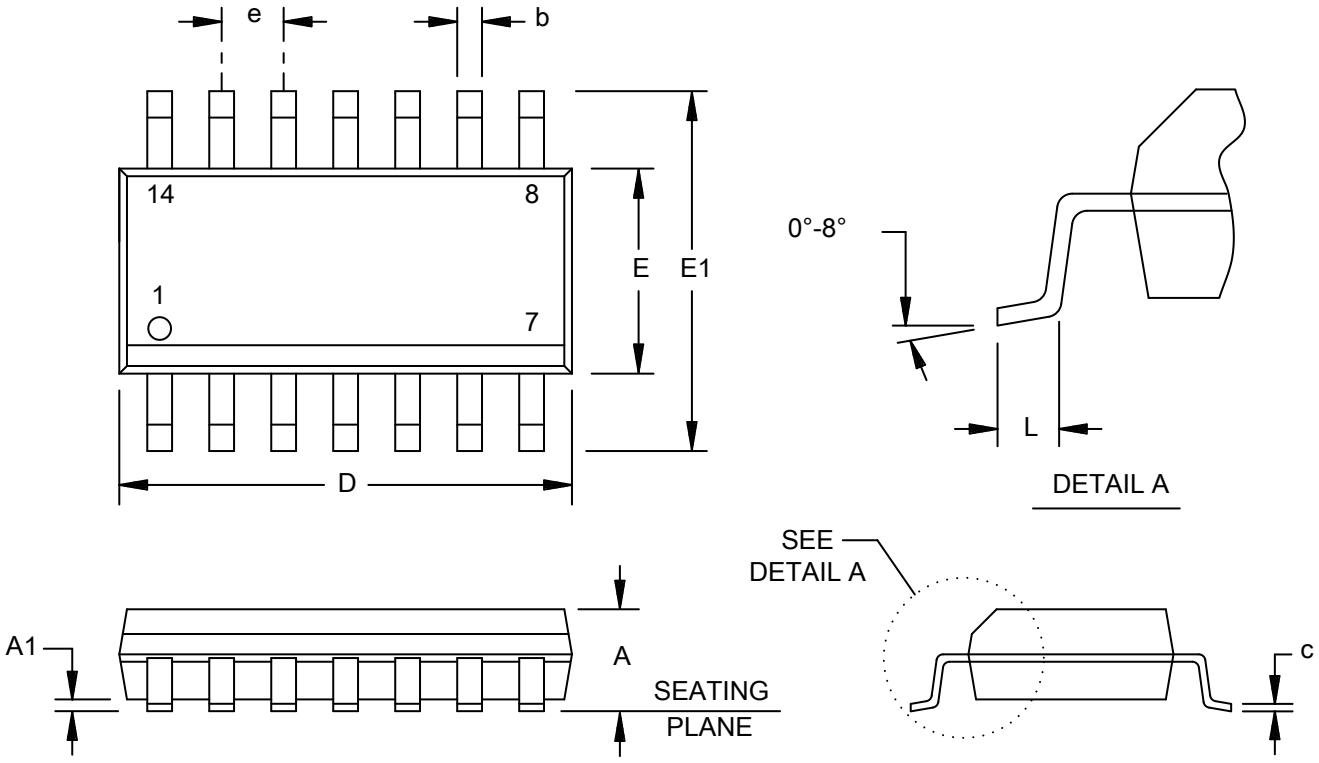
See footnote at end of table.

TABLE I. Electrical performance characteristics - Continued. 1/

Test	Symbol	Test conditions V_S = ±13 V, V_{CM} = 0 V T_A = 25°C unless otherwise noted	Limits			Unit
			Min	Typ	Max	
Input characteristics						
Offset voltage	V_{OS}			70	1000	µV
		-55°C < T_A < +85°C			1.8	mV
Input bias current	I_B			0.25	1	pA
		-55°C < T_A < +125°C			260	
Input offset current	I_{OS}				0.5	
		-55°C < T_A < +125°C			65	
Input voltage range			-13		+10	V
Common mode rejection ratio	CMRR	V_{CM} =-13 V to +10 V	90	107		dB
Large signal voltage gain	A_{VO}	R_L = 10 kΩ, V_O = -11 V to +11 V	215	290		V/mV
Offset voltage drift	$\Delta V_{OS}/\Delta T$	-55°C < T_A < +125°C		2.5		µV/°C
Output characteristics						
Output voltage high	V_{OH}		12.95			V
		I_L = 1 mA, -55°C to +125°C	12.94			
Output voltage low	V_{OL}				-12.95	
		I_L = 1 mA, -55°C to +125°C			-12.94	
Output current	I_{OUT}			±12		mA
Power supply						
Power supply rejection ratio	PSRR	V_S = ±2.5 V to ±13 V	90	107		dB
Supply current/Amplifier	I_{SY}			200	290	µA
		-55°C < T_A < +125°C			330	
Dynamic performance						
Slew rate	SR			3		V/µs
Gain bandwidth product	GBP			3.5		MHz
Phase margin	$ø_m$			60		Degrees
Noise performance						
Voltage noise	e_N p-p	f = 0.1 Hz to 10 Hz		4.2		µV p-p
Voltage noise density	e_N	f = 1 kHz		27.5		nV/√Hz
Current noise density	i_N	f = 1 kHz		0.5		fA/√Hz

1/ Testing and other quality control techniques are used to the extent deemed necessary to assure product performance over the specified temperature range. Product may not necessarily be tested across the full temperature range and all parameters may not necessarily be tested. In the absence of specific parametric testing, product performance is assured by characterization and/or design.

Case X



Dimensions									
Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	1.35	1.75	.053	.019	E	3.80	4.00	.150	.157
A1	0.10	0.25	.004	.010	E1	5.80	6.20	.228	.244
b	0.31	0.51	.012	.020	e	1.27 BSC		.050 BSC	
c	0.17	0.25	.012	.020	L	0.40	1.27	.016	.050
D	8.55	8.75	.337	.345					

NOTES:
1. Controlling dimensions are in millimeters; inch dimensions are rounded off millimeter equivalents for reference only and are not appropriate for use in design.
2. Falls within JEDEC MS-012-AB.

FIGURE 1. Case outline.

Case outline X			
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	OUT A	14	OUT D
2	-IN A	13	-IN D
3	+INA	12	+IN D
4	V+	11	V-
5	+IN B	10	+IN C
6	-IN B	9	-IN C
7	OUT B	8	OUT C

FIGURE 2. Terminal connections.

4. VERIFICATION

4.1 Product assurance requirements. The manufacturer is responsible for performing all inspection and test requirements as indicated in their internal documentation. Such procedures should include proper handling of electrostatic sensitive devices, classification, packaging, and labeling of moisture sensitive devices, as applicable.

5. PREPARATION FOR DELIVERY

5.1 Packaging. Preservation, packaging, labeling, and marking shall be in accordance with the manufacturer's standard commercial practices for electrostatic discharge sensitive devices.

6. NOTES

6.1 ESDS. Devices are electrostatic discharge sensitive and are classified as ESDS class 1 minimum.

6.2 Configuration control. The data contained herein is based on the salient characteristics of the device manufacturer's data book. The device manufacturer reserves the right to make changes without notice. This drawing will be modified as changes are provided.

6.3 Suggested source(s) of supply. Identification of the suggested source(s) of supply herein is not to be construed as a guarantee of present or continued availability as a source of supply for the item. DLA Land and Maritime maintains an online database of all current sources of supply at http://www.landandmaritime.dla.mil/Programs/Smcr/.

Vendor item drawing administrative control number 1/	Device manufacturer CAGE code	Vendor part number
V62/12653-01XE	24355	AD8643TRZ-EP-R7

1/ The vendor item drawing establishes an administrative control number for identifying the item on the engineering documentation.

CAGE code	Source of supply
24355	Analog Devices 1 Technology Way P.O. Box 9106 Norwood, MA 02062-9106